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DICKSTEIN SHAPIRO LLP
1825 EYE STREET, NW
WASHINGTON, DC 20006

EXAMINER	
BEMBEN, RICHARD M	

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2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/721,191	ALTICE ET AL.	
	Examiner	Art Unit	
	Richard M. Bemben	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) *1,2,11-20,33-43 and 46* is/are withdrawn from consideration.

5)☒ Claim(s) *7-9* is/are allowed.

6)☒ Claim(s) *3-5,10,21-23,25-32,44,45,47-49 and 51* is/are rejected.

7)☒ Claim(s) *6,27,50 and 54* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1, 2, 11-20 and 33-43, drawn to a CMOS image sensor where photosensors do not share floating diffusion (FD) nodes and reset circuitry, classified in class 348, subclass 302 & 308.

II. Claims 3-10, 21-32 and 45-51, drawn to a CMOS image sensor where photosensors share floating diffusion (FD) nodes and reset circuitry, classified in class 348, subclass 302 & 308.

The inventions are distinct, each from the other because of the following reasons:

2. **Inventions I and II** are directed to related CMOS image sensor. The related inventions are distinct if the (1) the inventions as claimed are either not capable of use together or can have a materially different design, mode of operation, function, or effect; (2) the inventions do not overlap in scope, i.e., are mutually exclusive; and (3) the inventions as claimed are not obvious variants. See MPEP § 806.05(j). In the instant case, **Inventions I and II** as claimed (1) are not capable of use together *and* have a materially different design (Figures 2-4 and 9-11), mode of operation (Figures 6-8), function and effect; (2) are mutually exclusive because of their materially different design and operation, such as the

additional capacitor required by **Invention II** at the FD node; and (3) the inventions are not obvious variants.

3. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions have acquired a separate status in the art due to their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

4. This application contains claims directed to the following patentably distinct species:

Species 1: Figures 3, 7 and 10 (claim 46) directed to 2 photosensors per FD node and reset circuitry

Species 2: Figures 4, 8 and 11 (claims 4, 6, 8 and 47) directed to 4 photosensors per FD node and reset circuitry

5. The species are independent or distinct because they at least have a material different design, mode of operation, and function.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, claims 3, 5, 7, 9, 10, 21-32, 44, 45 and 48-51 are generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added.

An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

6. During a telephone conversation with Jennifer McCue (Reg. No. 55,440) on 8 January 2008 a provisional election was made without traverse to prosecute **Invention II, Species 2**, claims 4, 6, 8 and 47 and generic claims 3, 5, 7, 9, 10, 21-32, 44, 45 and 48-51. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1, 2, 11-20 and 33-43 directed to **Invention I** and claim 46 directed to **Invention II, Species 1** are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

7. Applicant's election of **Invention II, Species 2** during the telephone conversation with Jennifer McCue (Reg. No. 55,440) on 8 January 2008 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

8. The abstract of the disclosure is objected to because in the "Brief Description of the Drawings" Figures 5-11 are mislabeled. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 22 recites the limitation "said floating diffusion node" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 3-5, 10, 21-23, 25-32, 44, 45, 47-49 and 51 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,693,670 issued to Stark.

Regarding **claim 3**, Stark discloses a method of operating a plurality of pixels of an image sensor (refer to Figures 2-4 and c. 8, ll. 11-13 where plural, e.g. 4, 6, 8 or 16, unit cells share floating diffusion node D (node near "107" in Figure 4) and read out circuitry) comprising:

accumulating a first charge in a first photosensor (individual sampling of unit photosensors, c. 7, l. 66 – c. 8, l. 5; c. 9, ll. 37-60; Figure 5);

transferring said first charge from said first photosensor to a first storage node within a first pixel (each photosensor has capacitor for storage - c. 8, ll. 52-64);

transferring said first charge from said first storage node to a floating diffusion node (c. 9, ll. 54-64);

reading out the first charge from said floating diffusion node as an output signal of said first pixel (c. 9, ll. 54-64);

accumulating a second charge in a second photosensor (same steps repeated for each photosensor - c. 9, l. 65 – c. 10, l. 3; Figure 5);

transferring said second charge from said second photosensor to a second storage node within a second pixel (each photosensor has capacitor for storage - c. 8, ll. 52-64);

transferring said second charge from said second storage node to said floating diffusion node (same steps repeated for each photosensor - c. 9, l. 65 – c. 10, l. 3; Figure 5); and

reading out the second charge from said floating diffusion node as an output signal of said second pixel (same steps repeated for each photosensor - c. 9, l. 65 – c. 10, l. 3; Figure 5).

Regarding **claim 4**, refer to the rejection of claim 3 and Stark further discloses sharing said floating diffusion node with a third and fourth pixel (Figures 2-4), wherein said floating diffusion node is reset, said third pixel accumulates a third charge in a third photosensor, transfers said third charge from said third photosensor to a third storage node within a substrate of said third pixel, transfers said third charge from said third storage node to said floating diffusion node and reads out the third charge from said floating diffusion node as an output signal of said third pixel (same steps repeated for each photosensor - c. 9, l. 65 – c. 10, l. 3; Figure 5); and

wherein said floating diffusion node is reset, said fourth pixel accumulates a fourth charge in a fourth photosensor, transfers said fourth charge from said fourth photosensor to a fourth storage node within a substrate of said fourth pixel, transfers said fourth charge from said fourth storage node to said floating diffusion node and reads out the fourth charge from said floating diffusion node as an output signal of said fourth pixel (same steps repeated for each photosensor - c. 9, l. 65 – c. 10, l. 3; Figure 5).

Regarding **claim 5**, refer to the rejection of claim 3 and Stark further discloses a readout circuit outputs the first and second charges by:

turning on a first transfer gate of the first pixel to transfer the first charge to the floating diffusion node (turning on 104A in Figure 4, analogous to description given in c. 9, ll. 37-45), providing an output signal based on charge at the floating diffusion node (Figure 4, node near "107") with an output transistor (c. 6, ll. 60; Figure 4, source follower buffer 108) and turning on a row select transistor (c. 6, ll. 55; Figure 4, readout transistor 30) to output a signal provided by said output transistor; and

turning on a second transfer gate of the second pixel after the readout of said first pixel to transfer the second charge to said floating diffusion node providing an output signal based on charge at the floating diffusion node with an output transistor, and turning on said row select transistor (same steps repeated for each photosensor - c. 9, l. 65 – c. 10, l. 3).

Regarding **claim 10**, Stark discloses a method of reading charge from pixels of an image sensor comprising:

turning on a first transfer gate transistor associated with a first pixel to transfer a first charge from a storage node within a substrate of said first pixel to a floating diffusion node (c. 9, ll. 37-45; Figure 5);

providing an output signal of said first pixel from said first charge stored in said floating diffusion node (c. 9, ll. 45-53; Figure 5);

turning on a row select transistor to output said first pixel output signal (c. 9, ll. 54-64; Figure 5);

turning on a second transfer gate transistor associated with a second pixel to transfer a second charge from a storage node within said second pixel to said floating diffusion node (same steps repeated for each photosensor - c. 9, l. 65 – c. 10, l. 3; Figure 5);

providing an output signal of said second pixel from said second charge stored in said floating diffusion node (same steps repeated for each photosensor - c. 9, l. 65 – c. 10, l. 3; Figure 5); and

turning on a row select transistor connected to the floating diffusion node to output said second pixel output signal (same steps repeated for each photosensor - c. 9, l. 65 – c. 10, l. 3; Figure 5).

Regarding **claim 21**, Stark discloses a pixel circuit comprising:

a plurality of photosensors for accumulating charge (photosensitive portion of 102A-D, Figure 4; also refer to c. 2, l. 66 – c. 3, l. 18);

a plurality of first transistors for transferring charge from a respective one of said photosensors to a respective first storage node (c. 8, ll. 52-64; Figure 4, 102A-D; also refer to c. 2, l. 66 – c. 3, l. 18);

a plurality of second transistors for transferring charge from said respective first storage node to a respective second storage node (Figure 4, 104A-D, floating diffusion region near "107"); and

a readout circuit for providing a pixel output signal based on charges transferred to said respective second storage node (c. 6, ll. 54-62; Figure 4, reset transistor 26, source follower buffer 108 and readout transistor 30).

Regarding **claim 22**, refer to the rejection of claim 1 and Stark further discloses that said readout circuit further comprises a reset transistor connected to said floating diffusion node for resetting the voltage on the floating diffusion node prior to receiving charge from a respective one said plurality of transfer gates (Figure 4, reset transistor 26 source (or drain) diffusion area is the floating diffusion area "107").

Regarding **claim 23**, refer to the rejection of claim 21 and Stark further discloses that the first storage nodes are formed within said pixel (c. 8, ll. 52-64).

Regarding **claim 25**, refer to the rejection of claim 21 and Stark further discloses that said first transistors operate as electronic shutters for said pixel circuit (first transistor transfers charge to its own associated capacitor in order for the integration time of all of the photosensors in a "cluster" are equal, acting as an electronic shutter – c. 8, ll. 52-64).

Regarding **claim 26**, refer to the rejection of claim 21 and Stark further discloses that the first transistor remain on during the integration period (photosensor is part of first transistor, therefore it is inherent that it remains on; Figure 4, 102A-D).

Regarding **claim 28**, refer to the rejection of claim 21 and Stark further discloses that said pixel circuit is a CMOS pixel (c. 1, ll. 27-40; c. 3, ll. 64-67).

Regarding **claim 29**, refer to the rejection of claim 21 and Stark further discloses that said pixel circuit is a five transistor pixel (each "pixel" comprises transistors 102, 104, and shared transistors 26, 108 and 30 in Figure 4).

Regarding **claim 30**, Stark discloses a pixel circuit for use in an imaging device, said pixel circuit comprising:

a plurality of photosensors for generating charge during an integration period (photosensitive portion of 102A-D, Figure 4; also refer to c. 2, l. 66 – c. 3, l. 18);

a plurality of shutter transistors, each shutter transistor connected to and transferring charge from a respective photosensor (c. 8, ll. 52-64; Figure 4, 102A-D, transistors 102A-D transfer charge to own associated capacitors in order for the integration time of all of the photosensors in a "cluster" to be equal, acting as an electronic shutter; also refer to c. 2, l. 66 – c. 3, l. 18);

a plurality of storage nodes, each node connected to a respective shutter transistor and storing charge transferred by a respective one of said plurality of photosensors (each photosensor has capacitor for storage - c. 8, ll. 52-64; also refer to c. 2, l. 66 – c. 3, l. 18);

a plurality of transfer gates, each transfer gate connected to and transferring charge from a respective storage node (Figure 4, 104A-D);

a floating diffusion node connected to said plurality of transfer gates for receiving charge from said storage nodes (Figure 4, floating diffusion region near "107"); and

a readout circuit connected to said floating diffusion node to output charge accumulated at the floating diffusion node (c. 6, ll. 54-62; Figure 4, reset transistor 26, source follower buffer 108 and readout transistor 30).

Regarding **claim 31**, refer to the rejection of claim 30 and Stark further discloses that a plurality of pixel circuits share said floating diffusion node, reset transistor, source follower transistor, and row select transistor (shared transistors 26, 108 and 30 in Figure 4).

Regarding **claim 32**, refer to the rejection of claim 30 and Stark further discloses that said pixel circuit is a CMOS pixel (c. 1, ll. 27-40; c. 3, ll. 64-67).

Regarding **claim 44**, Stark discloses an imaging system comprising:

a processor (inherent, there must be some sort of processor in order to drive APS as seen in Figure 5);

an imaging device comprising an array of pixels, coupled to said imaging system and array comprising:

a plurality of photosensors for generating charge during an integration period (photosensitive portion of 102A-D, Figure 4; also refer to c. 2, l. 66 – c. 3, l. 18);

a plurality of shutter transistors, each shutter transistor connected to and transferring charge from a respective photosensor (c. 8, ll. 52-64; Figure 4, 102A-D, transistors 102A-D transfer charge to own associated capacitors in order for the integration time of all of the photosensors in a "cluster" to be equal, acting as an electronic shutter; also refer to c. 2, l. 66 – c. 3, l. 18);

a plurality of storage nodes, each node connected to a respective shutter transistor and storing charge transferred by a respective one of said plurality of photosensors (each photosensor has capacitor for storage - c. 8, ll. 52-64; also refer to c. 2, l. 66 – c. 3, l. 18);

a plurality of barrier regions, each barrier region separating a respective photosensor from its respective storage node (the storage nodes are capacitors formed in diffused region below the photogate as described in c. 2, l. 66 – c. 3, l. 18, it is inherent in a CMOS process that these diffused regions have some form of field oxide barrier in order to separate them from other diffused regions)

a plurality of transfer gates, each transfer gate connected to and transferring charge from a respective storage node (Figure 4, 104A-D);

a floating diffusion node connected to said plurality of transfer gates for receiving charge from said storage nodes (Figure 4, floating diffusion region near "107"); and

a readout circuit connected to said floating diffusion node to output charge accumulated at the floating diffusion node (c. 6, ll. 54-62; Figure 4, reset transistor 26, source follower buffer 108 and readout transistor 30).

Regarding **claim 45**, Stark discloses an imaging system comprising:

a processor (inherent, there must be some sort of processor in order to drive APS as seen in Figure 5); and

an imaging device comprising an array of pixels, coupled to said imaging system said array comprising:

a plurality of photosensors for accumulating charge (photosensitive portion of 102A-D, Figure 4; also refer to c. 2, l. 66 – c. 3, l. 18);

a plurality of first transistors for transferring charge from a respective one of said photosensors to a respective first storage node (c. 8, ll. 52-64; Figure 4, 102A-D, transistors 102A-D transfer charge to own associated capacitors; also refer to c. 2, l. 66 – c. 3, l. 18);

a plurality of second transistors for transferring charge from said respective first storage node to a respective second storage node (Figure 4, 104A-D); and

a readout circuit for providing a pixel output signal based on charges transferred to said respective second storage node (c. 6, ll. 54-62; Figure 4, reset transistor 26, source follower buffer 108 and readout transistor 30).

Regarding **claim 47**, refer to the rejection of claim 45 and Stark further discloses that a number of said plurality of photosensors is four photosensors (102A-D, Figure 4).

Regarding **claim 48**, refer to the rejection of claim 45 and Stark further discloses that said first transistor is an electronic shutter (c. 8, ll. 52-64; Figure 4, 102A-D, transistors 102A-D transfer charge to own associated capacitors in order for the integration time of all of the photosensors in a "cluster" to be equal, acting as an electronic shutter; also refer to c. 2, l. 66 – c. 3, l. 18).

Regarding **claim 49**, refer to the rejection of claim 45 and Stark further discloses that the first transistor remains on during the integration period (photosensor is part of first transistor, therefore it is inherent that it remains on; Figure 4, 102A-D).

Regarding **claim 51**, refer to the rejection of claim 45 and Stark further discloses that said imaging system is a CMOS imaging system (c. 1, ll. 27-40; c. 3, ll. 64-67).

Allowable Subject Matter

13. Claims 7-9 are allowed.

14. The following is an examiner's statement of reasons for allowance: In a CMOS APS having plural photosensors, starting to read a second photosensor charge into a floating diffusion area while reading out a first photosensor charge from said floating diffusion area, i.e. while row select transistor remains on, could not be found in the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

15. Claims 6, 24, 27 and 50 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references disclose APS comprising plural photosensitive elements sharing floating diffusion regions and readout circuitry:

U.S. Patent No. 7,244,918 issued to McKee et al.

U.S. Patent No. 7,238,926 issued to Guidash et al.

U.S. Patent No. 7,064,362 issued to Roy

U.S. Patent No. 7,053,947 issued to Sohn

U.S. Patent No. 6,867,806 issued to Lee et al.

U.S. Patent No. 6,750,912 issued to Tennant et al.

U.S. Patent No. 6,731,335 issued to Kim et al.

U.S. Patent No. 6,657,665 issued to Guidash

U.S. Patent No. 6,486,913 issued to Afghahi et al.

U.S. Patent No. 6,352,869 issued to Guidash

U.S. Patent No. 6,107,655 issued to Guidash

U.S. Patent No. 6,043,478 issued to Wang

U.S. Pub. No. 2005/0012836 to Guidash

U.S. Pub. No. 2005/0248675 to Hashimoto et al.

U.S. Pub. No. 2002/0018131 to Kochi

U.S. Pub. No. 2001/0006402 to Hoiser et al.

The following references disclose APS comprising electronic shutters:

U.S. Patent No. 6,522,357 issued to Beiley et al.

U.S. Pub. No. 2001/0007471 to Beiley

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard M. Bemben whose telephone number is (571) 272-7634. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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LIN YE
SUPERVISORY PATENT EXAMINER